TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. BU998062

In Re Application Of: **Dean et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/394,302	September 10, 1999	Chu, Gabriel L.	2184

Invention: **BUILT-IN APPLICATION SPECIFIC INTEGRATED CIRCUIT IN-TRANSIT TEST SYSTEM**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Dean et al.

Serial No. 09/394,302 Group Art Unit: 2184

Filed: September 10, 1999 Examiner: Chu, Gabriel L.

For: BUILT-IN APPLICATION SPECIFIC INTEGRATED CIRCUIT IN-TRANSIT TEST SYSTEM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' APPEAL BRIEF

Sirs:

Appellants respectfully appeal the final rejection of claims 55-70 in the Office Action dated October 27, 2003. A Notice of Appeal was timely filed on January 23, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corp., Armonk, New York, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 55-70 are all the claims pending in the application and are set forth fully in the attached appendix. Claims 1-54 were originally filed in the application. Claims 1-54 were cancelled, and claims 55-83 were added in an Amendment filed on December 3, 2002. Claims 71-83 were cancelled in an Amendment filed April 29, 2003. Claims 84-96 were added in an Amendment filed on September 17, 2003. Claims 84-96 were cancelled in an Amendment filed December 19, 2003.

IV. STATEMENT OF AFTER-FINAL AMENDMENTS

An after-final Amendment filed on December 19, 2003 cancelled claims 84-96. An Advisory Action dated January 15, 2003 indicated that, upon filing an appeal, the Amendment filed on December 13, 2003 did not place the application in condition for allowance, but would be entered for the purposes of appeal. The Advisory Action further stated that the rejection of claims 55-70 would remain. The claims shown in the appendix are shown in their amended form as of the December 19, 2003 Amendment.

V. SUMMARY OF THE INVENTION

As shown in Appellants' Figure 1, the claimed invention comprises an in-transit test box 10 in which a plurality of test boards 11 are mounted. Appellants' Figure 3 illustrates one of the test boards that includes a number of sockets adapted to hold integrated circuit chips. The invention provides the benefit of eliminating chip tests at the receiving site because the parts are tested during the transit stage. Upon unpacking the chips, only fully tested/passing chips would be used for the next phase of card assembly.

Further, with the invention, more test patterns can be applied than would be allowed during the normal manufacturing process. Currently, the test time for each chip cannot be long, since the parts need to be shipped to the customer as soon as possible.

However, since testing with the invention is done in transit which can be hours (or even days), more chip test time is available, so many more patterns can be applied and test coverage correspondingly increased. Also different temperature/voltage combinations may be used, so that once the parts reach the final destination, the modules have had far more rigorous testing. This results in higher reliability, reduces in house manufacturing test time and reduces the overall cost by reducing the need for manufacturing testers.

VI. ISSUES PRESENTED FOR REVIEW

The issues presented for review by the Board of Patents Appeals and Interferences are whether claims 55-69 stand rejected under 35 U.S.C. §103(a) over Steiner (US Patent No. 4,291,404) in view of Miller et al. (US Patent No. 6,452,411) hereinafter Miller; and whether claim 70 stands rejected under 35 U.S.C. §103(a) over Steiner in view of Miller et al. and further in view of Roy et al. (US Patent No. 6,499,121).

VII. GROUPING OF THE CLAIMS

As supported by the following arguments, the claims are each independently patentable and do not stand or fall together. More specifically, the dependent claims are patently distinct from the independent claims from which they depend because each dependent claim defines additional features which are not defined in the independent claims or which are defined more broadly in the independent claims. As discussed in greater detail below, the features defined by the dependent claims are not merely illustrations or examples but include patentable features which prevent the dependent claims from standing or falling with their associated independent claim.

VIII. ARGUMENT

As explained in greater detail below, Appellants appreciate the Examiner's desire to succinctly categorize the claimed invention as a combination of two concepts, testing and portability; however, the invention is more than just a portable testing device.

Instead, the invention is designed to test integrated circuit chips while they are being transported to increase manufacturing efficiency by allowing longer testing times and by testing devices during a period of time when the devices would otherwise sit idle. Therefore, the claims define structural features that relate to such transportation based testing (e.g., a transportable test box, a power supply in the test box, test boards having multiple sockets in the test box, etc.) that would not have been obvious given the teachings of Steiner, Miller, and Roy.

Roy and Miller teach parallel testing of multiple chips using a known good chip, as well as across-device and within-device testing. Steiner teaches a portable testing device used to test individual chips in the field. The combination of Steiner with Roy and/or Miller is problematic because modifying Steiner to allow the testing of multiple chips in parallel destroys its ability to remain easily portable. The advantages of the structure in Steiner are its small size, light weight, and low-power consumption that allow it to be easily carried by a service technician to perform in-field testing at remote locations. Modifying Steiner to perform simultaneous testing of multiple chips would increase its size, weight, and power consumption and destroy its intended function. Therefore, it is initially argued below that a *prima facia* case of obviousness has not been set forth.

Further, even if one ordinarily skilled in the art had made the combination proposed in the Office Action, there still is no teaching of the transportable test box, or a power supply within such a test box. To the contrary, the most that such a combination can teach is a portable self-powered test board for simultaneously testing multiple chips (using a known good die, cross-check testing, and within-chip testing). More specifically, the portable device described in Steiner can only be described as a test board in that the portable test device includes sockets on the exterior to which integrated circuit chips are to be attached. There is no concept in the prior art of record of a box that would surround and protect such a test board (or multiple test boards as in the claims) in-transit, or of a power supply that is located within such a box.

Appellants strongly disagree with the conclusion reached in the Office Action that the term "transported" can be any form of movement no matter how small, because this diverges substantially from the plain meaning of the claim language and from the

intended use of the portable testing device disclosed in Steiner. More specifically, Steiner clearly explains that the "portability" feature of its testing apparatus relates to the ability to transport the test apparatus to the device under test to allow a field technician to travel to a defective device and test individual chips that are removed from such a device. There is no conceptual teaching of utilizing the portable testing device in Steiner for the purpose of testing devices while they are being transported. Therefore, Steiner is devoid of teaching a structure for accomplishing this purpose, including the test box in which various test boards and a power supply are positioned.

While Appellants agree that the language of claims being examined should be provided with their broadest reasonable interpretation so as to insure adequate examination and the production of high quality patents, in this instance it is Appellants' position that the Examiner's interpretation of the term "transported" is unreasonable and diverges from the overall context of the structure being defined in the claims and the invention described in the specification. In other words, while a chip may be placed on the portable testing device of Steiner and that testing device can be moved, such disclosure does not teach the "transportable test box" defined in the claims because, given the overall context of the claims and the proper reading of the claim language in light of the specification, the term "transportable" in this situation clearly defines a structure that is designed to test integrated circuit chips when they are being transported from one location to another. This is conceptually different than movement of a portable testing device during the time when a technician in the field is attempting to diagnose a defective device. Simply put, Steiner is devoid of any concept similar to the type of transportation being defined in the claims. Thus, it is Appellants' position that Steiner does not teach or suggest the transportable structure defined by Appellants' claims.

For these and other reasons that are detailed below, Appellants submit that the claimed invention is patentable over the applied prior of record

A. The 103(a) Rejection Based on Steiner in view of Miller

1. The Position in the Office Action

Referring to claim 55, the Office Action states the following:

Steiner discloses a transportable circuit chip test device comprising: a transportable test box (See figure 1.); a test board in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated... "), wherein said test board comprises: a socket adapted to hold integrated circuit chips to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.). Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Referring to claim 56, the Office Action states the following:

Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant

combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

Referring to claim 57, the Office Action states the following:

Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated.

Referring to claim 58, the Office Action states the following:

Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et at., Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value, This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 59, the Office Action states the following:

Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

Referring to claim 60, the Office Action states the following:

Steiner in combination with Miller et al. disclose each of said test boards includes comparators electrically connected to said sockets (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 61, the Office Action states the following:

Steiner in combination with Miller et al. disclose said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)."), and wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 62, the Office Action states the following:

Steiner in combination with Miller et al. disclose said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously (From the technical field of Miller et al., "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel.").

Referring to claim 63, the Office Action states the following:

Steiner discloses a transportable integrated circuit (IC) chip test device, said device comprising: a transportable test box (See figure 1.); a test board mounted in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, 'A battery operated.., "), wherein said test board comprises: sockets adapted to hold an IC chip to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.). Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s} the throughput of the test system in terms of the number of DUTs tested per unit time". Further, although Steiner does not specifically disclose the comparison of a plurality of ICs, it is known in the art. An example of this is further shown by Miller et al. Miller et al. disclose said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said IC chips simultaneously, and wherein said testing circuitry identifies a defective IC chip as one having a different output when compared to outputs of the other ASIC chips, when all IC chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number

of devices in parallel." Wherein a faulty circuit's output is different.). A person of ordinary skill in the art at the time of the invention would have been motivated to compare DUTs in a portable tester because, from line 24 of column 1, "the manufacturer expects each constituent IC device to be virtually free of defects and to perform according to its specifications" Further, although Steiner does not specifically disclose the test device is adapted to test application specific integrated circuits (ASICs), the testing of ICs that are application specific is well known in the art. An example of this is an ASIC tester. A person of ordinary skill in the art at the time of the invention would have been motivated to test ASICs because they can be faulty.

Referring to claim 64, the Office Action states the following:

Steiner in combination with Miller et al. disclose all of said ASIC chips have an identical design (From line 6 of column 3, "As briefly summarized above, an embodiment of the invention provides for more efficient testing of a number of similar, and preferably identical, IC devices in parallel without altering the test program or the conventional tester.").

Referring to claim 65, the Office Action states the following:

Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the DUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

Referring to claim 66, the Office Action states the following:

Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery Operated ").

Referring to claim 67, the Office Action states the following:

Steiner in combination with Miller et al, disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 68, the Office Action states the following:

Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al. "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

Referring to claim 69, the Office Action states the following:

Steiner in combination with Miller et al. disclose all of said comparators are connected to known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding

locations in the DUTs and expected responses obtained form the KGO.").

2. Appellants' Position

a. Independent Claims 55 and 63

i. No *Prima Facia* Case of Obviousness

Initially, Appellants submit that the Office Action does not set forth a *prima facia* case of obviousness. The Office Action admits that Steiner does not disclose that the test board can hold more than one integrated circuit chip; however, the Office Action makes reference to Miller as showing test boards that hold multiple chips. However, Appellants respectfully submit that modifying the device in Steiner to hold multiple chips would destroy the operational functionally of the device in Steiner. More specifically, column 2, lines 10-49 of Steiner explain that the primary purpose of the single-chip test device is to provide a miniaturized hand-held battery operated field testing device that minimizes the memory space required and that prolongs battery life. Having multiple sockets and the ability to test multiple chips would destroy this functionality by making the device excessively large and making the device high in power consumption.

The device disclosed in Steiner was designed to be able to evaluate a chip during an in-field test procedure where a non-functional product is being tested at a remote location (see column 2, lines 4-9). Therefore, if a service technician were to suspect that a certain integrated circuit chip was defective, he could remove the chip from the non-functional product in question and individually test the chip using the device disclosed in Steiner. There would be little or no advantage in providing the device shown in Figure 1 of Steiner with the ability to test multiple chips because the diagnostic methods performed by field technicians generally evaluate each component individually so as to sequentially eliminate the potential causes of a defective condition. Once again, providing multiple sockets would merely make the device larger and make the device consume more power, which are contrary to the goals stated in Steiner of providing a

small, light weight, low power consumption hand-held device utilized for in-field testing by field technicians.

The device described in Miller is utilized during the manufacturing stage when many of the same devices are produced and where simultaneous testing of an identical devices increases testing efficiency. The device in Miller is provided with a continuous power supply and is not concerned with limiting the power consumption during testing. In addition, the size of the device in Miller does not need to be limited because it is not portable. Because of these differences, one ordinarily skilled in the art would not have been motivated to use the teachings of Miller in combination with the teachings of Steiner. For example, column 2, lines 1-3 of Steiner explains that large testing devices used during manufacturing (such as that disclosed in Miller) are impractical for use in field maintenance work. Therefore, Steiner created a device that was intentionally different than the device in Miller. Modifying the device to be larger and less practical for field maintenance work destroys the primary function of the device in Steiner. Thus, one ordinarily skilled in the art would not have modified the device in Steiner as suggested in the Office Action.

Miller relates to non-portable manufacturing environment with unlimited power supply, while Steiner relates to an in-field testing unit that has a limited power supply and is limited by size and weight constraints. Because of these differences, Appellants submit that is improper to combine the teachings of Steiner with those of Miller because the references come from such divergent testing environments and because there is no motivation in either reference to make the combination proposed in the Office Action.

Miller teaches parallel testing of multiple chips using a known good chip. Steiner teaches a portable testing device used to test individual chips in the field. The combination of Steiner with Miller is problematic because modifying Steiner to allow the testing of multiple chips in parallel destroys its ability to remain easily portable. The advantages of the structure in Steiner are its small size, light weight, and low-power consumption, which allow it to be easily carried by a service technician to perform in-field testing at remote locations. Modifying Steiner to perform simultaneous testing of multiple chips would increase its size, weight, and power consumption and destroy its

intended function. Therefore, it is initially argued that a *prima facia* case of obviousness has not been set forth.

ii. Prior Art Does Not Teach or Suggest the Claimed Invention

Steiner only shows a test board and not a box for holding boards, much less a power supply in the box for powering the boards. As mentioned above, the invention is more than just a portable testing device. Instead, the invention is designed to test integrated circuit chips while they are being transported to increase manufacturing efficiency by allowing longer testing times and by testing devices during a period of time when the devices would otherwise sit idle. Therefore, the claims define structural features that relate to such transportation based testing (e.g., a transportable test box, a power supply in the test box, test boards having multiple sockets in the test box, etc.) that would not have been obvious given the teachings of Steiner and Miller.

Miller teaches parallel testing of multiple chips using a known good chip. Steiner teaches a portable testing device used to test individual chips in the field. As shown above, it is initially argued below that a *prima facia* case of obviousness has not been set forth. Further, even if one ordinarily skilled in the art had made the combination proposed in the Office Action, there still is no teaching of the transportable test box, or a power supply within such a test box. To the contrary, the most that such a combination can teach it is a hand-held portable self-powered test board for simultaneously testing multiple chips (using a known good die). More specifically, the portable device described in Steiner can only be described as a test board in that the portable test device includes sockets on the exterior to which integrated circuit chips are to be attached. There is no concept in the prior art of record of a box in which the test board is located that would protect such a test board (or multiple test boards as in the claims) in-transit, or of a power supply that is located within such a box.

Appellants strongly disagree with the conclusion reached in the Office Action that the term "transported" can be any form of movement no matter how small because this diverges substantially from the plain meaning of the claim language and from the

intended use of the portable testing device disclosed in Steiner. More specifically, Steiner clearly explains that the "portability" feature of its testing apparatus relates to the ability to transport the test apparatus to the device under test to allow a field technician to travel to a defective device and test individual chips that are removed from such a device (col. 2, lines 35-39). There is no conceptual teaching of utilizing the portable testing device in Steiner for the purpose of testing devices while they are being transported. Therefore, Steiner is devoid of teaching a structure for accomplishing this purpose including the test box in which various test boards and a power supply are positioned.

While Appellants agree that the language of the claims being examined should be provided with their broadest reasonable interpretation so as to insure adequate examination and the production of high quality patents, in this instance it is Appellants' position that the Examiner's interpretation of the term "transported" is unreasonable and diverges from the overall context of the structure being defined in the claims and the invention described in the specification. In other words, while a chip may be placed on the portable testing device of Steiner and that testing device can be moved, such disclosure does not teach the "transportable test box" defined in the claims because, given the overall context of the claims and the proper reading of the claim language in light of the specification, the term "transportable" in this situation clearly defines a structure that is designed to test integrated circuit chips when they are being transported from one location to another. This is conceptually different than movement of a portable testing device during the time when a technician in the field is attempting to diagnose a defective device. Simply put, Steiner is devoid of any concept similar to the type of transportation being defined in the claims. Thus, it is Appellants position that Steiner does not teach or suggest the transportable structure defined by Appellants' claims.

As shown in Appellants' Figure 1, the claimed invention comprises a test box 10 in which a plurality of test boards 11 are mounted. Appellants' Figure 3 illustrates one of the test boards that includes a number of sockets adapted to hold integrated circuit chips. The Office Action proposes that Figure 1 of Steiner discloses a test box and that Figure 2 of Steiner discloses a test board. However, Appellants respectfully submit that Steiner only discloses a battery powered single chip test board and does not disclose any form of an in-transit test box for holding test boards.

More specifically, column 3, lines 11-24 of Steiner explain that Figure 1 shows a device for testing a chip and column 4, lines 37-42 explain that Figure 2 of Steiner illustrates the same device in a schematic format. Therefore, Appellants submit that Figures 1 and 2 do not illustrate a test box and test boards as proposed in the Office Action, but instead only illustrate at most a chip test board. In Figure 1 of Steiner, openings 10 are holes for receiving a dual in-line package (DIP), buttons 11-13 are user operation buttons, and item 16 is a display. The same items are shown in Figure 2. Therefore, Appellants submit that it is clear that Figures 1 and 2 illustrate the same device and that Steiner does not teach any form of a test box that is designed to hold test boards as in the invention defined by independent claims 55 and 63.

In addition, neither Miller nor Steiner describes testing circuitry that operates while in transit. Miller provides a fixed testing apparatus that is immovable and cannot be used in-transit. Steiner describes an in-field test device that is designed to be hand-held and used by a field technician when repairing a non-operating product. There is no suggestion in Steiner that the device could test a chip while being transported. Instead, such a scenario is only proposed in the Office Action as occurring when the portable test device of Steiner is moved (however so slightly). Therefore, Appellants respectfully submit that there is no teaching or suggestion of a device where the testing circuitry operates while in transit.

Thus, as shown above, many aspects of the invention defined by independent claims 55 and 63 are not taught or suggested by the prior art references. No reference teaches "a transportable test box". The references are not properly combinable to make the single-chip testing device in Steiner capable of testing multiple devices. Therefore, the references do not teach or suggest that "each of said test boards comprises: sockets." In addition, there is no teaching of performing the testing of the chips while in transit, or as defined by independent claims 55 and 63, there is no teaching of any device "adapted to hold integrated circuit chips to be tested while being transported." Therefore, Appellants respectfully submit that independent claims 55 and 63 are patentable over the proposed combination of references.

In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

b. The Independent Patentability of Dependent Claims 56-62 and 64-70

The following discussion demonstrates that the combination of Steiner in view of Miller does not teach or suggest the invention defined by the dependent claims, but also that the dependent claims are independently patentable over their associated independent claims and do not stand or fall with their associated independent claims.

Dependent claims 56 and 65 define that the test boards include visual test failure indicators, such that one of the visual test failure indicators is adjacent each of the sockets. As shown above, there is no teaching or suggestion in the prior art of record of any test board for use within an in-transit test box as in the claimed invention. Therefore, it is axiomatic that the prior of record cannot show such a test board that utilizes visual test indicators that allow the individual unpacking the in-transit test box to recognize immediately which chips did not pass the in-transit test procedures. Thus, any combination of Miller and Steiner would not teach or suggest the invention defined by dependent claims 56 and 65 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claims 56 and 65 are independently patentable over the applied prior art references on their own.

With respect to dependent claims 57 and 66, that define that portable power supply comprises a battery, once again, there is no teaching or suggestion the prior art of record of the inventive in-transit test box and, therefore, there can be no teaching of the inventive power supply within the in-transit test box (much less a teaching that this power supply could comprise a battery). Thus, any combination of Miller and Steiner would not teach or suggest the invention defined by dependent claims 57 and 66 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claims 57 and 66 are independently patentable over the applied prior art references on their own.

Dependent claims 58 and 67 define that each of the test boards includes a memory adapted to store test results. As mentioned above, there is no teaching or suggestion in

the prior art of record of any test board for use within an in-transit test box as in the claimed invention. Therefore, the prior of record cannot show such a test board that utilizes a memory adapted to store test results that allow the individual unpacking the in-transit test box to know immediately the test results of the chips stored during the in-transit test procedures. Thus, any combination of Miller and Steiner would not teach or suggest the invention defined by dependent claims 58 and 67 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claims 58 and 67 are independently patentable over the applied prior art references on their own.

Dependent claims 59, 68, and 69 define all of the comparators are connected to the known good integrated circuit chip. As shown above, there is no teaching or suggestion in the prior art of record of any test board for use within an in-transit test box as in the claimed invention. Therefore, the prior of record cannot show such a test board that utilizes a known good chip in the in-transit test procedures. Thus, any combination of Miller and Steiner would not teach or suggest the invention defined by dependent claims 59 and 68 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claims 59 and 68 are independently patentable over the applied prior art references on their own.

Dependent claim 60-62 defines each of the test boards includes comparators electrically connected to the sockets. As shown above, there is no teaching or suggestion in the prior art of record of any test board for use within an in-transit test box as in the claimed invention. Therefore, it is axiomatic that the prior of record cannot show such a test board that utilizes comparators in the in-transit test procedures. Thus, any combination of Miller and Steiner would not teach or suggest the invention defined by dependent claims 60-62 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claims 60-62 are independently patentable over the applied prior art references on their own.

Dependent claim 64 defines that all of the ASIC chips have an identical design and claim 70 defines that by comparing whether outputs of all ASIC chips are identical, the testing circuitry does not require a specific proper output that a given input should

produce for the specific design of ASIC chip being tested. Once again, there is no teaching or suggestion in the prior art of record of any test board for use within an in-transit test box as in the claimed invention. Therefore, the prior of record cannot show such a test board that compares the similarity of identically designed ASIC chip outputs to recognize immediately which chips is defective. Thus, any combination of Miller and Steiner would not teach or suggest the invention defined by dependent claims 64 and 70 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claims 64 and 70 are independently patentable over the applied prior art references on their own.

Thus, as shown above, dependent claims 56-62 and 64-70 are similarly patentable not only by virtue of their dependency from a patentable independent claim but also by virtue of the additional features of the invention they define. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

B. The 103(a) Rejection Based on Steiner, Miller, and Roy

1. The Position in the Office Action

Referring to claim 70, the Office Action states the following:

> Although Steiner in combination with Miller et al. do not specifically disclose by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested, testing without a known output is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs.
>
> In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If

desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into a portable circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus Promoting a more efficient testing methodology."

2. Appellants' Position

a. Independent Claims 55 and 63

i. No *Prima Facia* Case of Obviousness

The Office Action makes reference to Roy for teaching comparing outputs of ASIC chips to identify defective chips. However, it is Applicants' position that Roy is

not properly combinable with Steiner for the same reasons that Miller was not properly combinable with Steiner. Therefore, Applicants again submit that a *prima facia* case of obviousness has not been set forth.

More specifically, Roy is not directed to a portable device, nor is Roy directed to a device utilized for in-field testing. Roy presents a large device for testing multiple ASIC chips simultaneously given very little space and power restrictions. Combining Roy with Steiner would destroy the portability and low-power consumption functionality of the hand-held device in Steiner. Further, Steiner relates to in-field testing devices, while Roy relates to a testing device to be used during manufacturing. There is no motivation within any of the references for making the proposed combination.

Therefore, the teachings of Roy are not properly combinable with the teachings of Steiner. Thus, it is Applicants' position that the references are not properly combinable to teach the features defined by dependent claim 70.

ii. Prior Art Does Not Teach or Suggest the Claimed Invention

Roy it is substantially similar to Miller except that instead of teaching the use of a known good chip, Roy utilizes cross-device and within-device testing. Indeed, Roy and Miller were related applications and filed on the same day. Therefore, Roy adds very little to the previous discussion and the reasoning stated above the also applies here.

Therefore, it is again Applicants' position that many aspects of the invention defined by independent claim 63 are not taught or suggested by the prior art references. No reference teaches "a transportable test box." The references are not properly combinable to make the single-chip testing device in Steiner capable of testing multiple devices. Therefore the references do not teach or suggest that "each of said test boards comprises: sockets." In addition, there is no teaching of performing the testing of the chips while in transit, or as defined by independent claim 63, there is no teaching of any device "adapted to hold integrated circuit chips to be tested while being transported." Therefore, Applicants respectfully submit that independent claim 63 is patentable over the proposed combination of references. Further, it is Applicants position' that dependent

claims 70 is similarly patentable and that this rejection should be removed. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

b. The Independent Patentability of Dependent Claim 70

The following discussion demonstrates that the combination of Steiner and Miller in further view of Roy does not teach or suggest the invention defined by the dependent claim 70, but also that the dependent claims are independently patentable over their associated independent claims and do not stand or fall with their associated independent claims.

Dependent claim 70 defines that by comparing whether outputs of all ASIC chips are identical, the testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested. Once again, there is no teaching or suggestion in the prior art of record of any test board for use within an in-transit test box as in the claimed invention. Therefore, the prior of record cannot show such a test board that compares the similarity of identically designed ASIC chip outputs to recognize immediately which chips are defective. Thus, no combination of Steiner, Miller, and/or Roy would not teach or suggest the invention defined by dependent claim 70 which indicates that these features are novel and are independently patentable over their respective independent claims. Therefore, dependent claim 70 is independently patentable over the applied prior art references on its own.

Thus, as shown above, dependent claim 70 is patentable, not only because it depends from a patentable independent claim, but also because of the additional features the dependent claim defines. In view the foregoing, the Board is respectfully requested to reconsider and withdraw this rejection.

IX. CONCLUSION

The invention is designed to test integrated circuit chips while they are being transported to increase manufacturing efficiency by allowing longer testing times and by testing devices during a period of time when the devices would otherwise sit idle. The

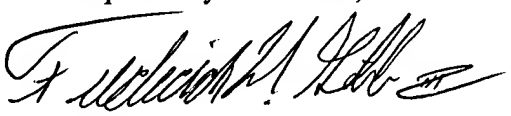
claims define structural features that relate to such transportation based testing (e.g., a transportable test box, a power supply in the test box, test boards having multiple sockets in the test box, etc.) that would not have been obvious given the teachings of Steiner, Miller, and/or Roy.

Roy and Miller teach parallel testing of multiple chips using a known good chip, as well as across-device and within-device testing. Steiner teaches a portable testing device used to test individual chips in the field. The combination of Steiner with Roy and/or Miller is problematic because modifying Steiner to allow the testing of multiple chips in parallel destroys its ability to remain easily portable. The advantages of the structure in Steiner are its small size, light weight, and low-power consumption that allow it to be easily carried by a service technician to perform in-field testing at remote locations. Modifying Steiner to perform simultaneous testing of multiple chips would increase its size, weight, and power consumption and destroy its intended function. Therefore, it is initially argued below that a *prima facia* case of obviousness has not been set forth.

Further, even if one ordinarily skilled in the art had made the combination proposed in the Office Action, there still is no teaching of the transportable test box, or a power supply within such a test box. To the contrary, the most that such a combination can teach is a portable self-powered test board for simultaneously testing multiple chips (using a known good die, cross-check testing, and within-chip testing). More specifically, the portable device described in Steiner can only be described as a test board in that the portable test device includes sockets on the exterior to which integrated circuit chips are to be attached. There is no concept in the prior art of record of a box that would surround and protect such a test board (or multiple test boards as in the claims) in-transit, or of a power supply that is located within such a box.

In view the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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APPENDIX

1-54. (Cancelled)

55. (Previously Presented) A transportable integrated circuit chip test device comprising:

a transportable test box;

a plurality of test boards mounted in said test box; and

a portable power supply in said test box connected to said test boards,

wherein each of said test boards comprises:

sockets adapted to hold integrated circuit chips to be tested while being transported; and

testing circuitry electrically connected to said sockets.

56. (Previously Presented) The device in claim 55, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

57. (Previously Presented) The device in claim 55, wherein said portable power supply comprises a battery.

58. (Previously Presented) The device in claim 55, wherein each of said test boards includes a memory adapted to store test results.

59. (Previously Presented) The device in claim 55, wherein each of said test boards includes a known good integrated circuit chip.

60. (Previously Presented) The device in claim 59, wherein each of said test boards includes comparators electrically connected to said sockets.

61. (Previously Presented) The device in claim 60, wherein said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip, and

wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips.

62. (Previously Presented) The device in claim 61, wherein said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously.

63. (Previously Presented) A transportable integrated circuit chip test device adapted to test application specific integrated circuit (ASIC) chips, said device comprising:

a transportable test box;

a plurality of test boards mounted in said test box; and

a portable power supply in said test box connected to said test boards,

wherein each of said test boards comprises:

sockets adapted to hold ASIC chips to be tested while being transported; and

testing circuitry electrically connected to said sockets, wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said ASIC chips simultaneously, and

wherein said testing circuitry identifies a defective ASIC chip as one having a different output when compared to outputs of the other ASIC chips, when all ASIC chips are supplied with identical inputs.

64. (Previously Presented) The device in claim, 63 wherein all of said ASIC chips have an identical design.

65. (Previously Presented) The device in claim 63, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

66. (Previously Presented) The device in claim 63, wherein said portable power supply comprises a battery.

67. (Previously Presented) The device in claim 63, wherein each of said test boards includes a memory adapted to store test results.

68. (Previously Presented) The device in claim 63, wherein each of said test boards includes a known good integrated circuit chip.

69. (Previously Presented) The device in claim 68, wherein all of said comparators are connected to said known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip.

70. (Previously Presented) The device in claim 63, wherein by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested.

71-96. (Cancelled)